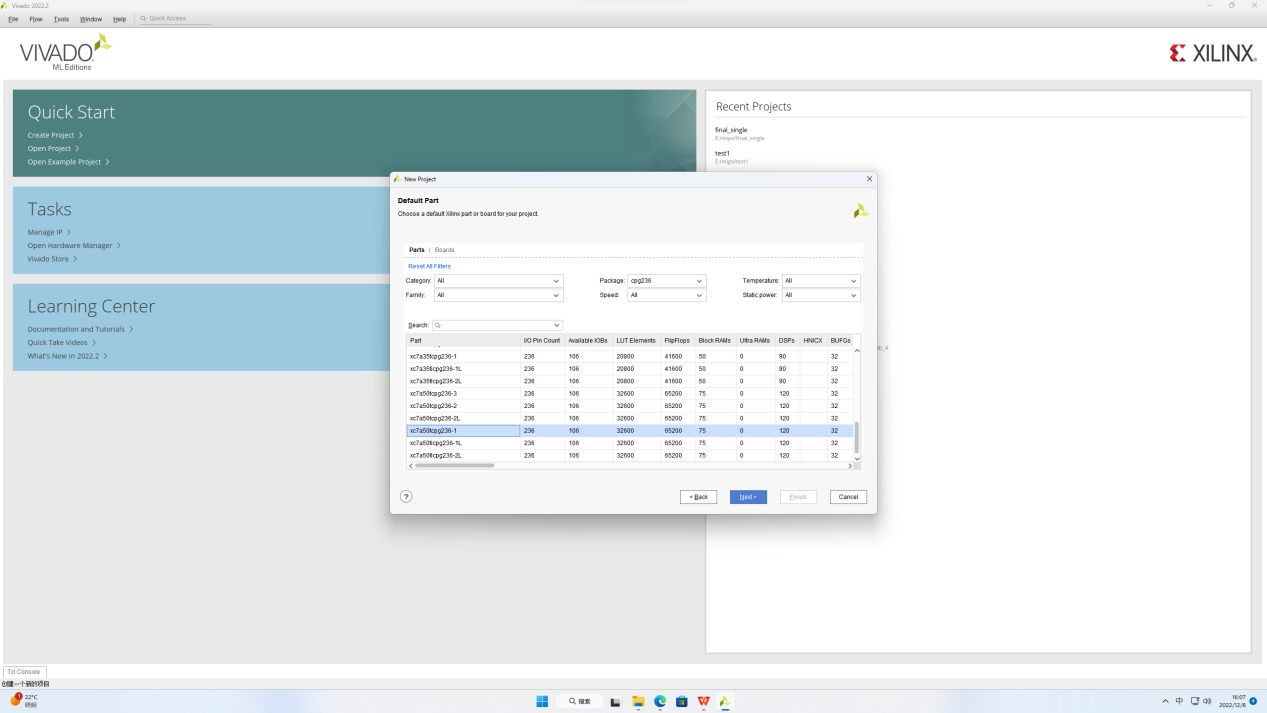
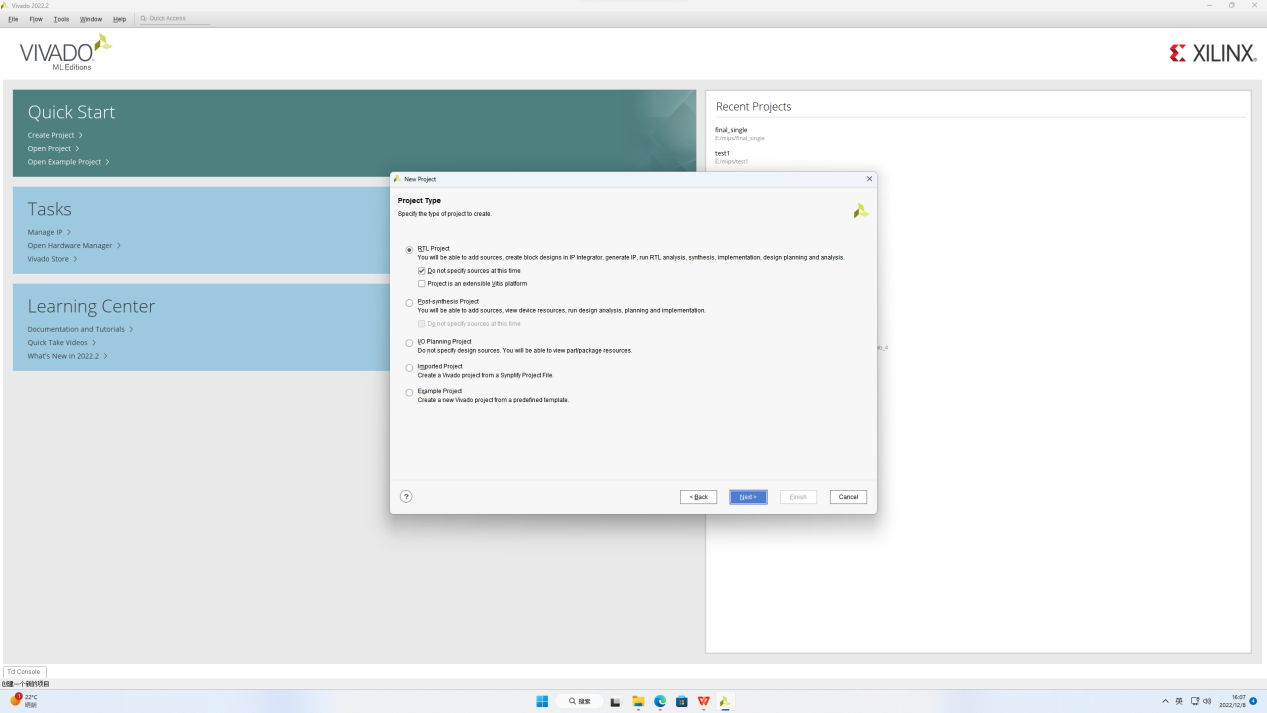
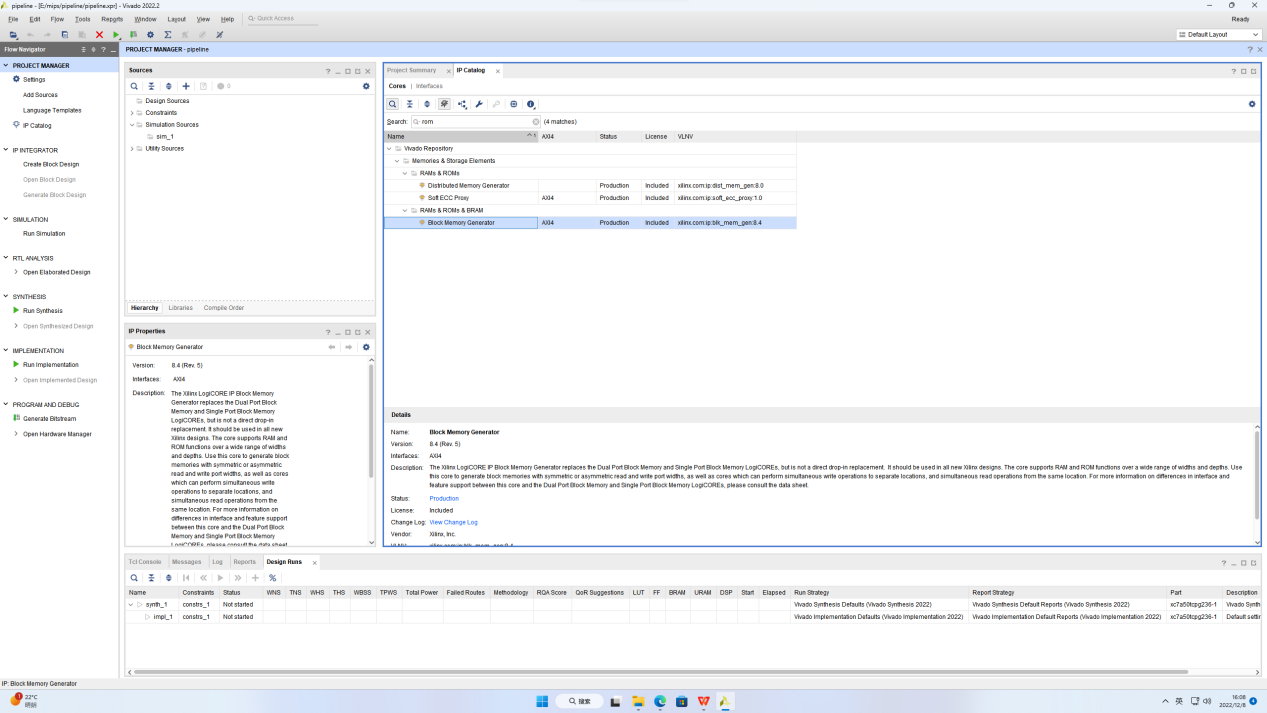
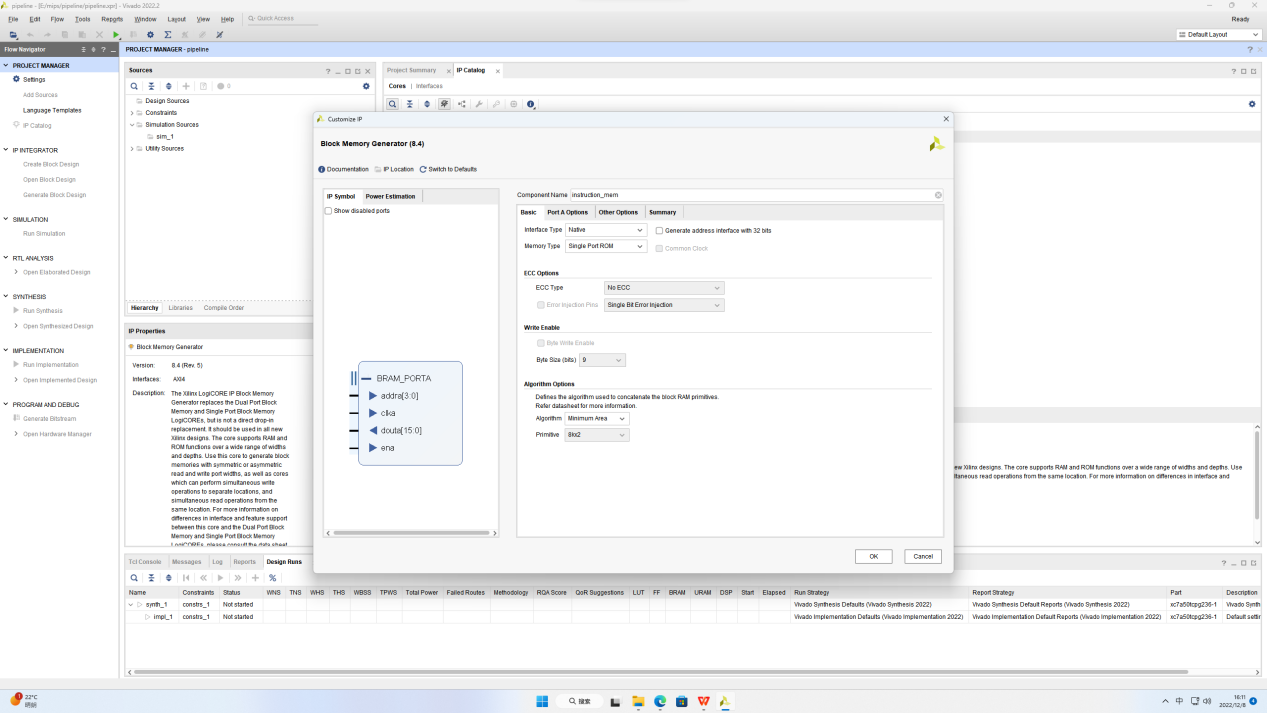
New project:



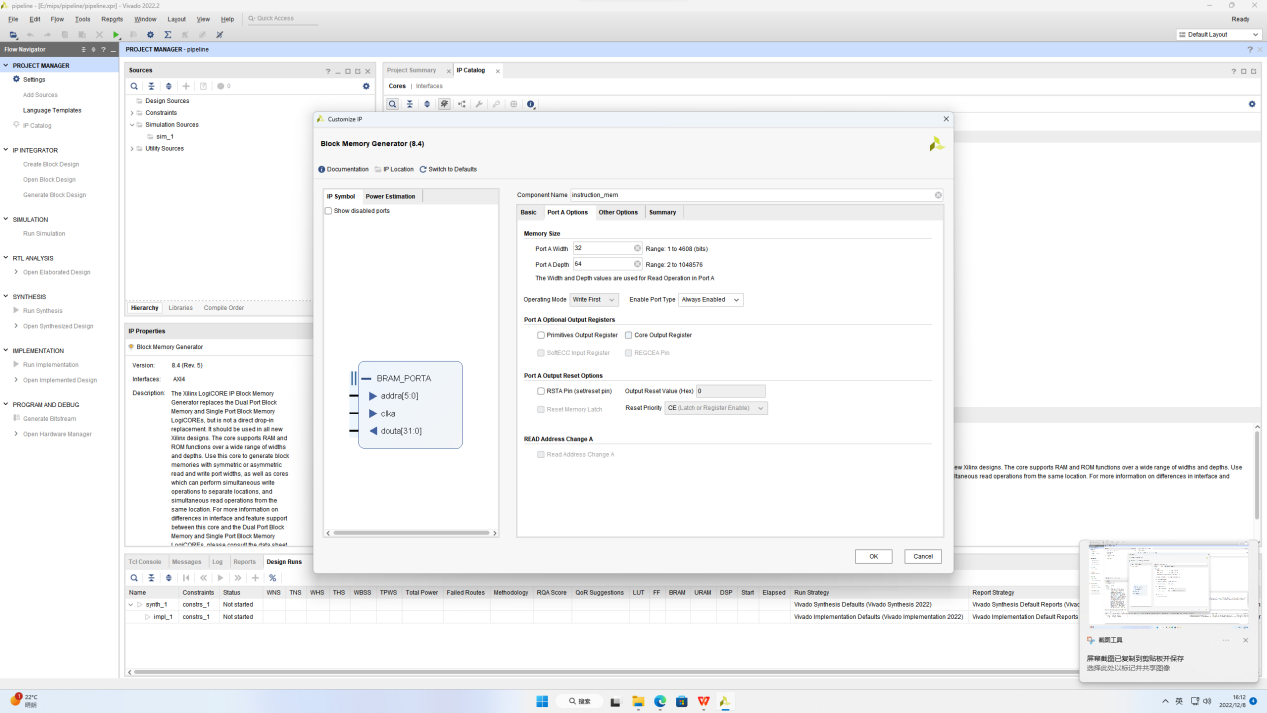
Generate IP CORE:

Instruction\_mem: use single port Rom because we use coe document to initialize instruction memory and there are no needs to write instruction\_mem;

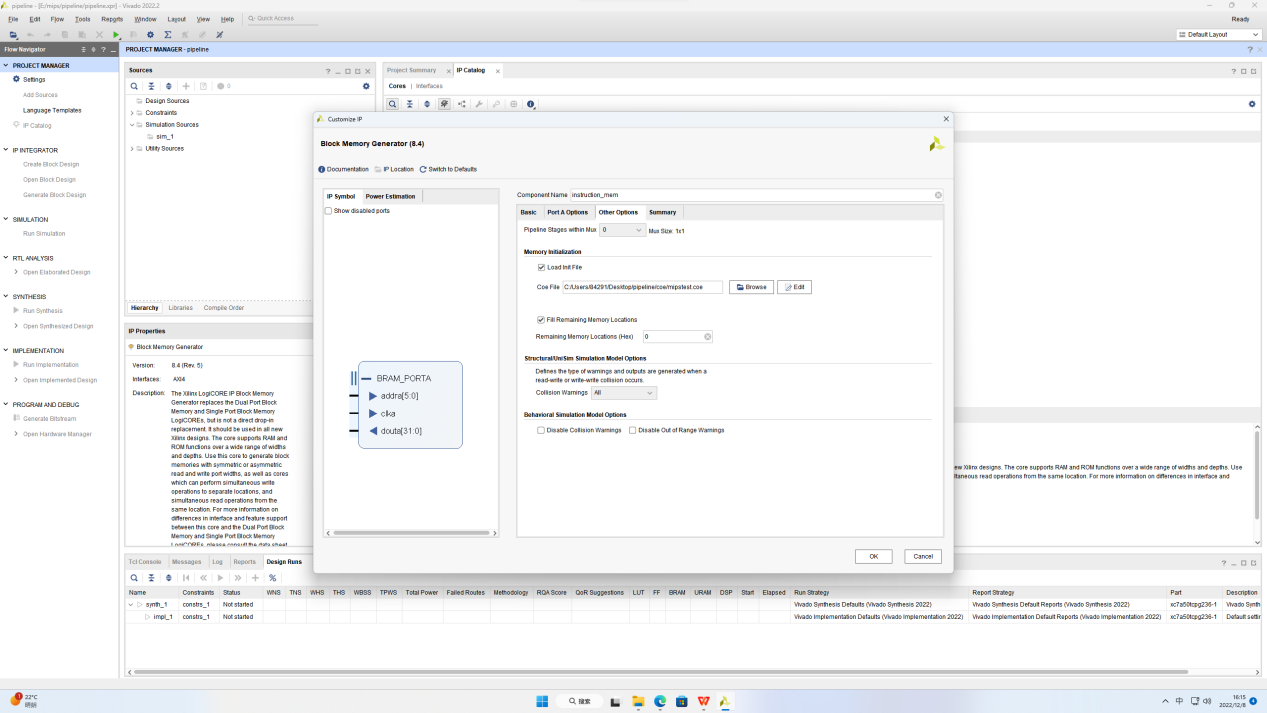


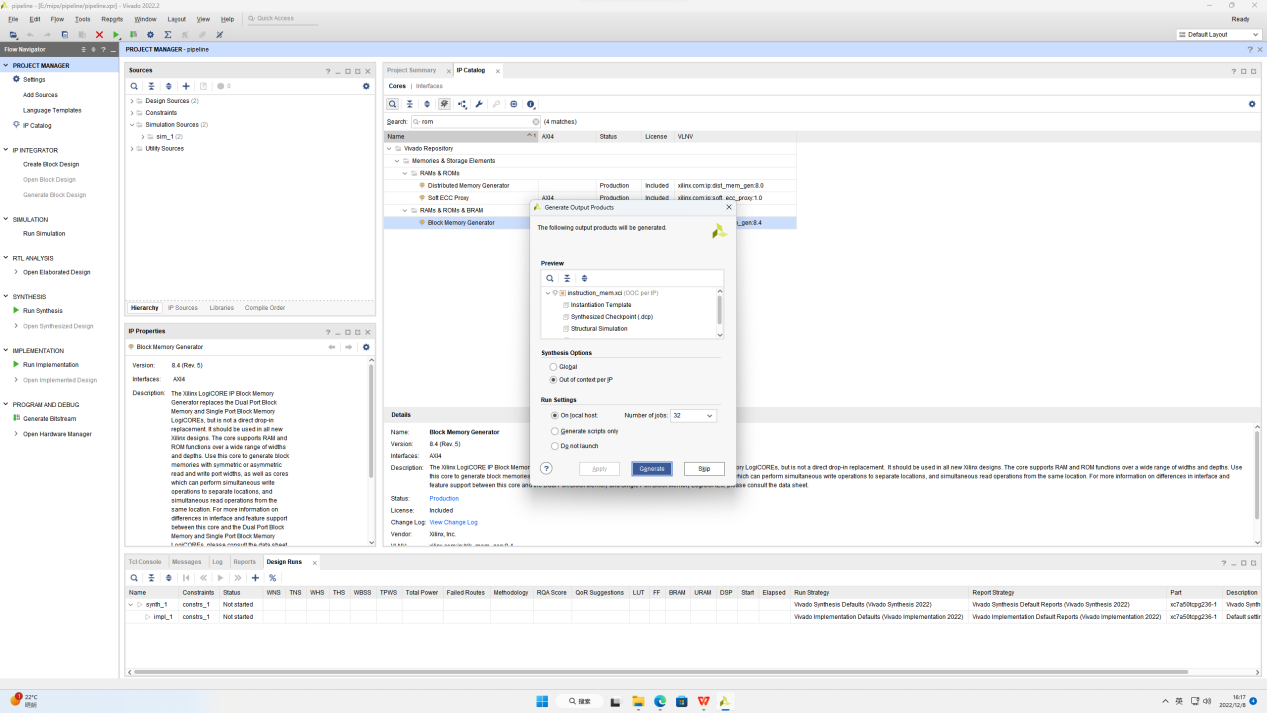


Don’t choose Primitives Output Register because this will make instruction\_mem take an extra cycle to output and we need to set the Enable Port Type to Always Enable thus reducing one of the required enable signals.

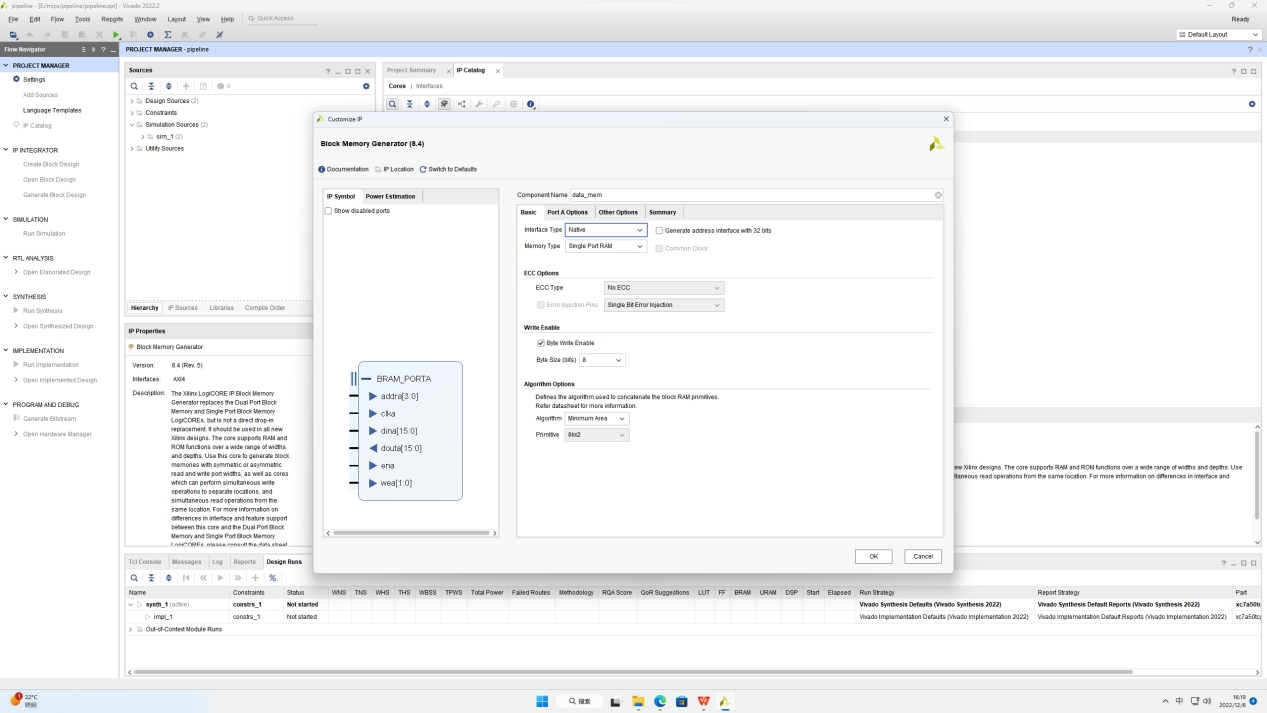


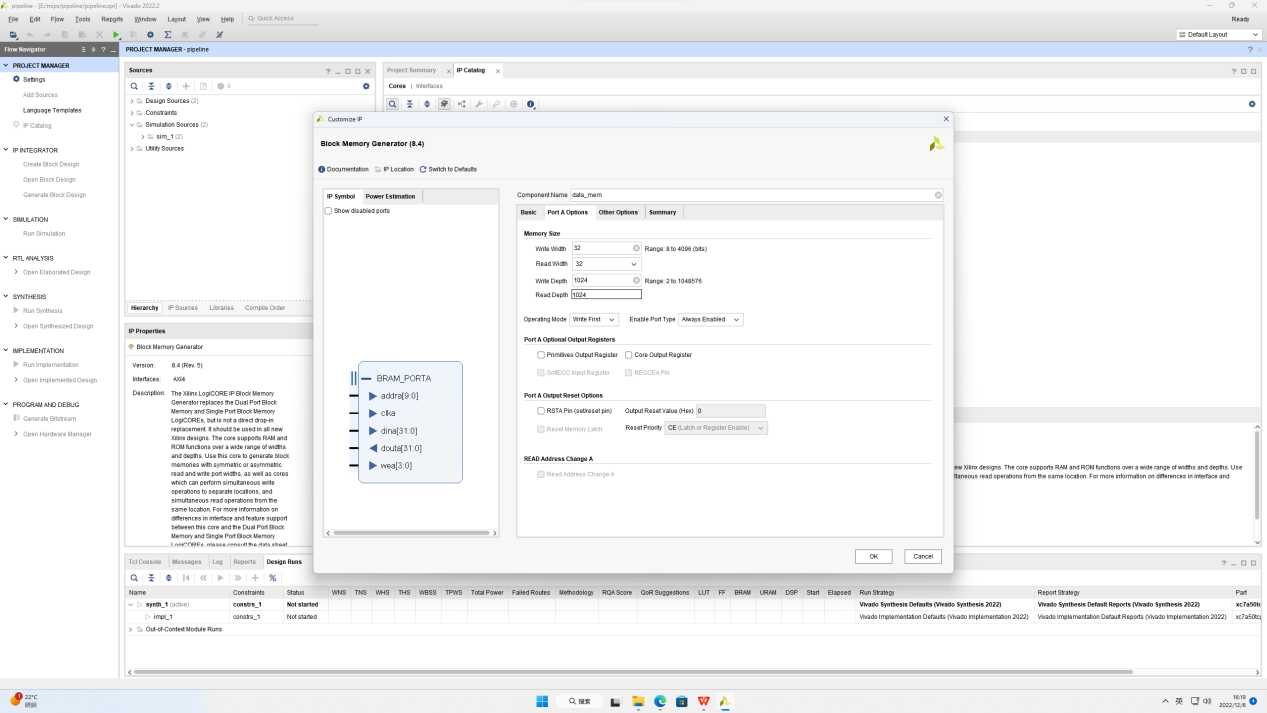
Load Init File using coe file;

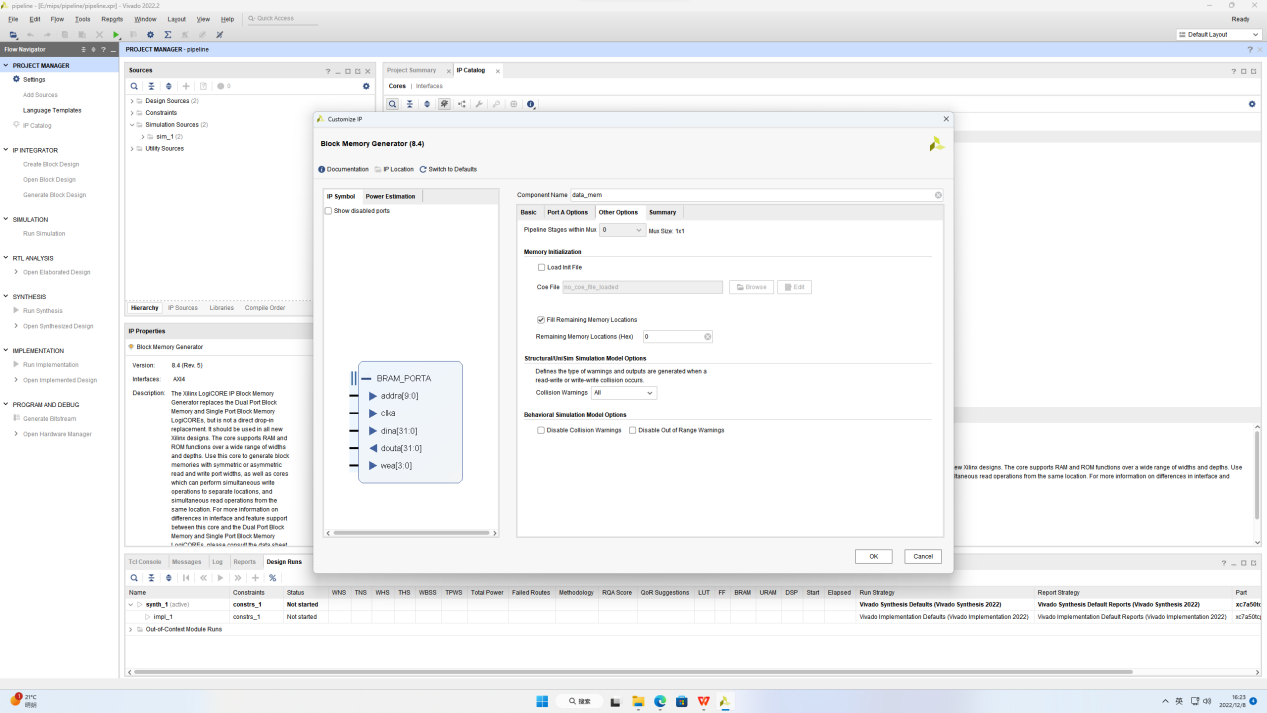




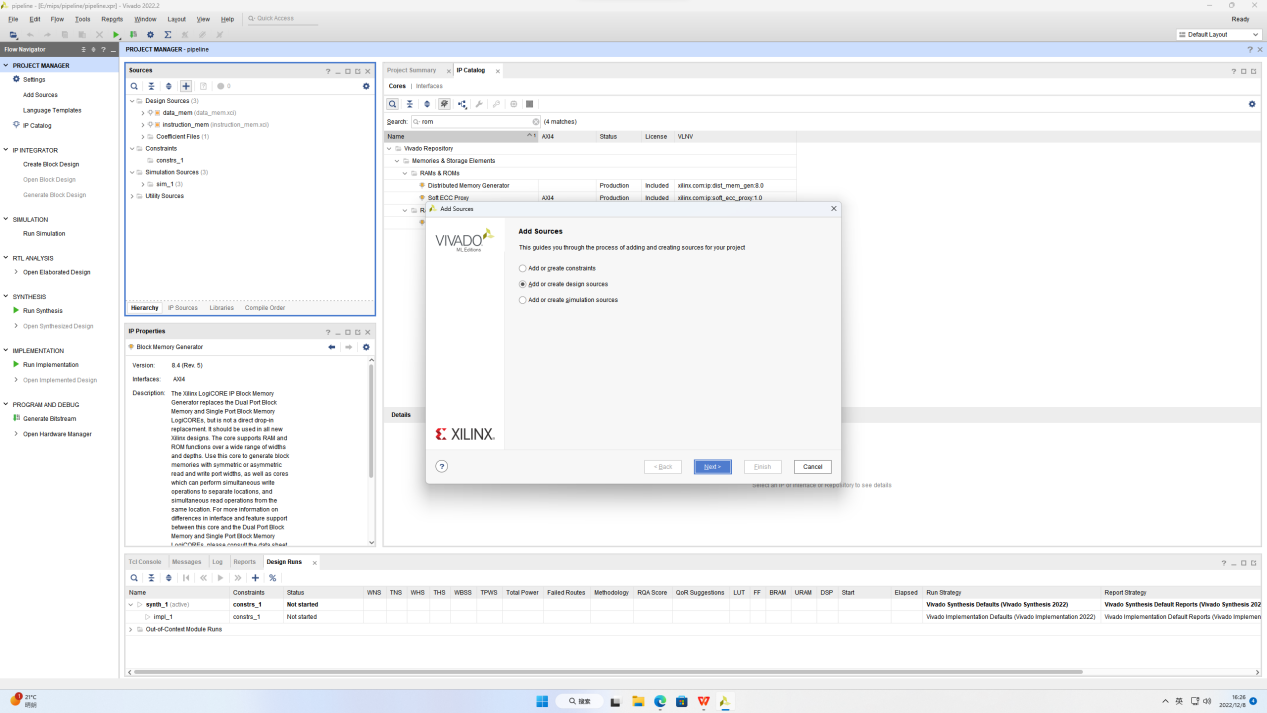
Data\_mem: Use single port ram because we need to write data\_mem;

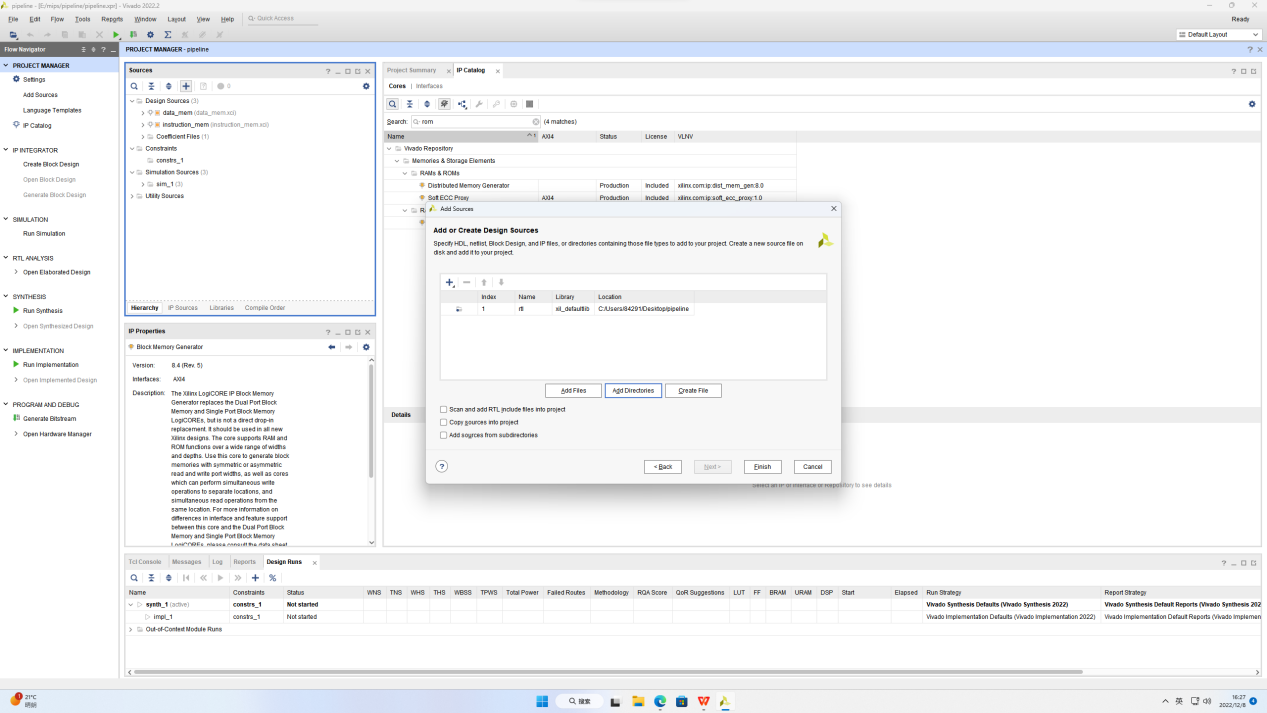






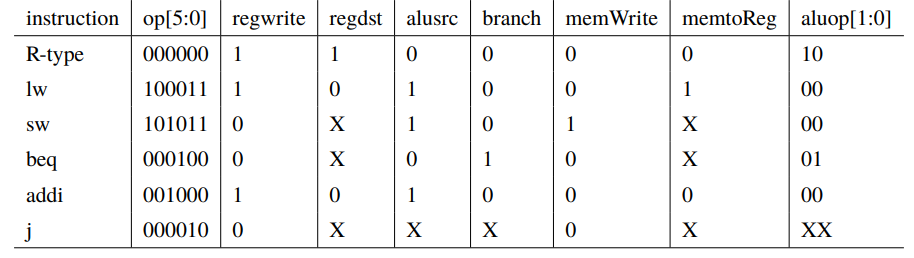
Add design source:



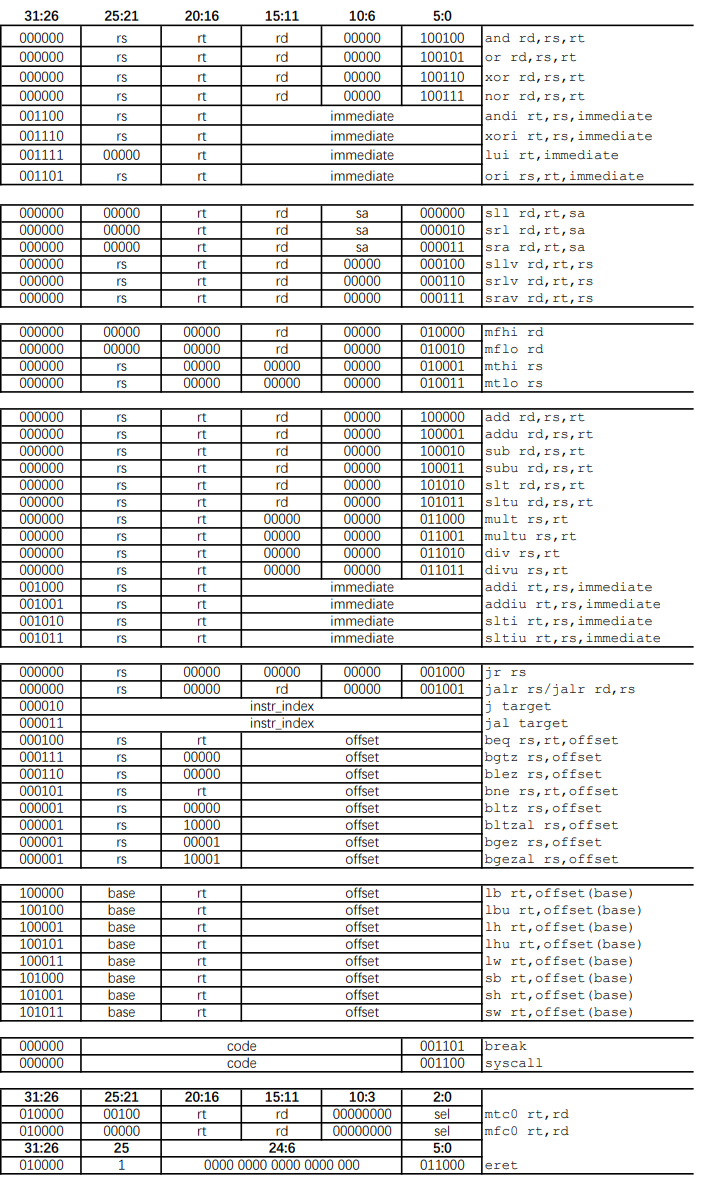


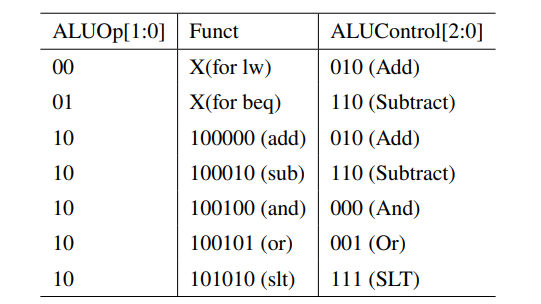
Alu and control:

The instructions involved:

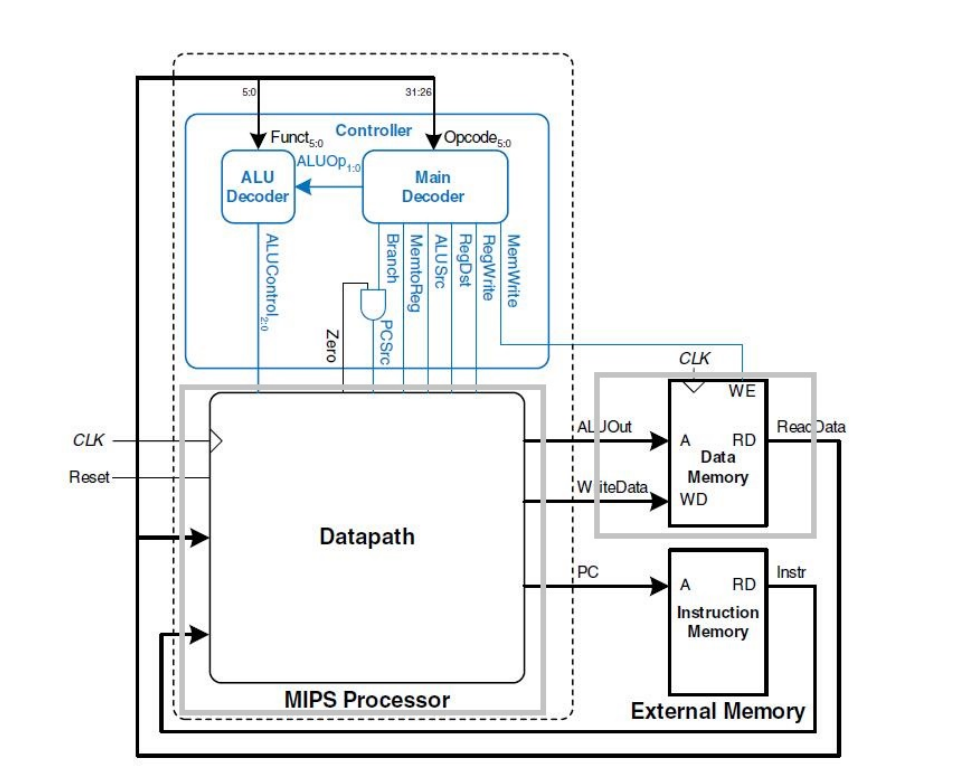


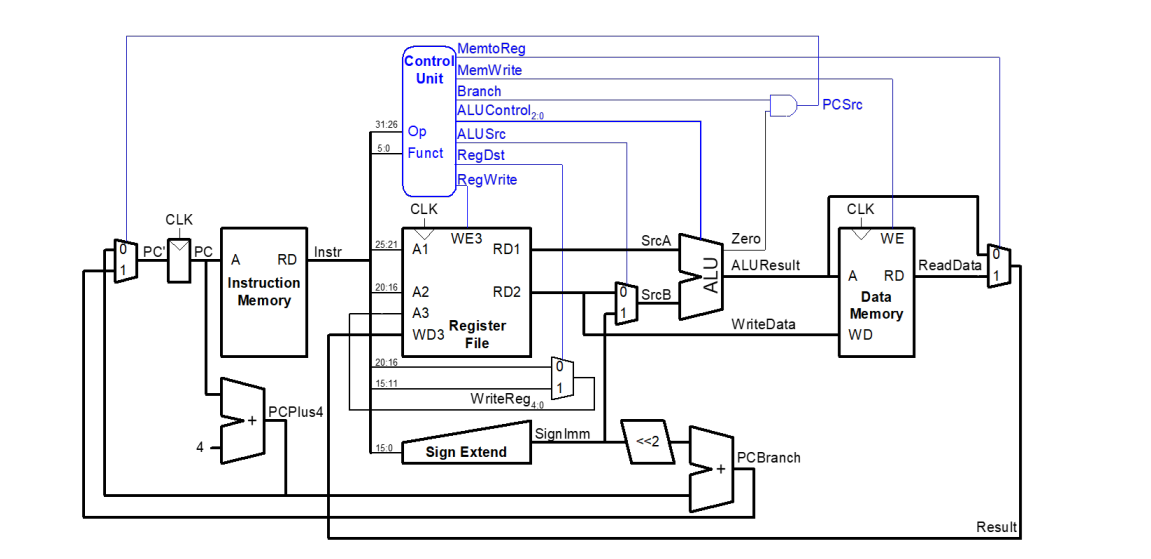
MIPS instruction machine code:

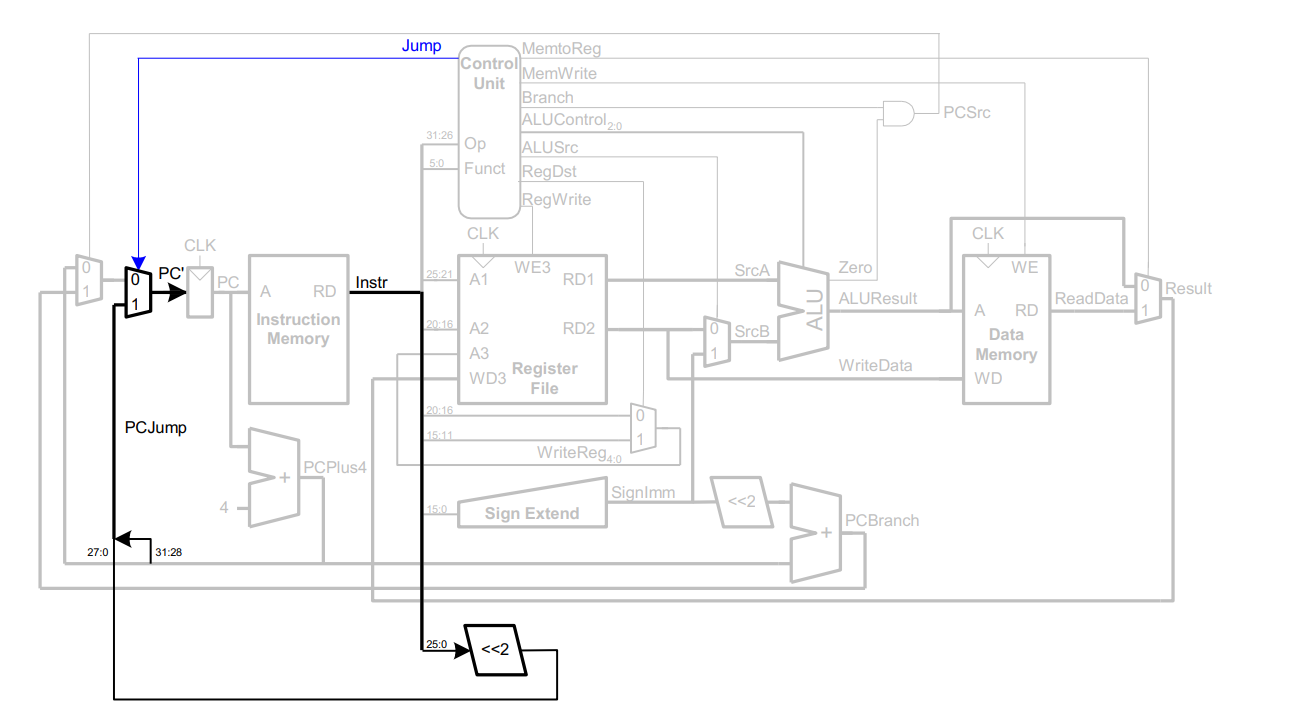




Single-cycle:







Single cycle to pipeline:

